

ABSTRACT

An image processing apparatus has an arithmetic circuit 20 for generating pixel data of output pixels by arithmetically processing the pixel data of M horizontally adjoining pixels and N vertically adjoining pixels. A first temporary storage section 21

5 readably stores the pixel data of the pixels ranging from the Mth pixel to the last pixel in each horizontal pixel line of an image. A second temporary storage section 22 readably stores the pixel data of the pixels ranging from the head pixel to the (M-1)th pixel in each horizontal pixel line of the image. A third temporary storage section 23

10 delays the pixel data stored in the first temporary storage section 21, receives the pixel data from the second temporary storage section 22, and simultaneously outputs pixel data of the M horizontally adjoining pixels and the N vertically adjoining pixels.